

CLAIMS

What is claimed is:

- 5 1. A method for forming a semiconductor device comprising:
 providing a semiconductor substrate;
 forming an insulating layer on a surface of the semiconductor
 substrate;
 providing a strained semiconductor layer on the insulating layer;
10 defining a <100> direction of the strained semiconductor layer; and
 forming a transistor on the strained semiconductor layer, wherein
 the transistor is aligned along the <100> direction of the
 strained semiconductor layer.
- 15 2. The method of claim 1, wherein the strained semiconductor layer is in a
 tensile stress state.
3. The method of claim 1, wherein providing a strained semiconductor layer
 further comprises:
20 providing an at least partially relaxed silicon-germanium layer on
 the insulating layer; and
 forming a silicon layer on the at least partially relaxed silicon-
 germanium layer to form the strained semiconductor layer.
- 25 4. The method of claim 1, wherein providing a strained semiconductor layer
 on the insulating layer comprises:
 forming a semiconductor layer on the insulating layer; and
 straining the semiconductor layer.

5. The method of claim 1, further comprising defining a $\langle 110 \rangle$ direction of the semiconductor substrate.

5 6. The method of claim 5, further comprising aligning the $\langle 110 \rangle$ direction with the $\langle 100 \rangle$.

7. A method for forming a semiconductor device comprising:

providing a semiconductor substrate;

10 defining a $\langle 110 \rangle$ direction of the semiconductor substrate;

forming an insulating layer on a surface of the semiconductor substrate;

providing a pre-strained semiconductor layer;

defining a $\langle 100 \rangle$ direction of the pre-strained semiconductor layer;

15 bonding the semiconductor layer to the insulating layer, wherein

the $\langle 100 \rangle$ of the pre-strained semiconductor layer is aligned with the $\langle 110 \rangle$ direction of the semiconductor substrate; and

forming a transistor on the pre-strained semiconductor layer,

20 wherein the transistor is aligned along the $\langle 100 \rangle$ direction of the pre-strained semiconductor layer.

8. The method of claim 7, wherein providing a pre-strained semiconductor layer further comprises:

providing an at least partially relaxed silicon-germanium layer; and

25 forming a silicon layer on the at least partially relaxed silicon-

germanium layer from the pre-strained semiconductor layer.

9. The method of claim 7, wherein the semiconductor device is characterized as being a silicon-on-insulator device.
10. The method of claim 7, wherein bonding of the pre-strained
5 semiconductor layer to the insulating layer is performed by thermal wafer bonding.
11. The method of claim 7, wherein forming a transistor on the pre-strained
10 semiconductor layer comprises aligning a source/drain axis of the transistor along the <100> direction of the pre-strained semiconductor layer.
12. The method of claim 7, wherein forming a transistor on the pre-strained
15 semiconductor layer comprises aligning a source/drain axis of the transistor perpendicular to the <100> direction of the pre-strained semiconductor layer.
13. The method of claim 7, further comprising cleaving the semiconductor
20 device through the pre-strained semiconductor layer.
14. The method of claim 13, further comprising removing the pre-strained
semiconductor layer after cleaving.
15. A method for forming a semiconductor device comprising:
25 providing a semiconductor substrate;
defining a crystal orientation of the semiconductor substrate;
forming an insulating layer on a surface of the semiconductor
substrate;

providing a pre-strained semiconductor layer;
defining a crystal orientation of the pre-strained semiconductor
layer;
bonding the pre-strained semiconductor layer to the insulating
5 layer, wherein the crystal orientation of the pre-strained
semiconductor layer is not aligned with the crystal
orientation of the semiconductor substrate; and
forming a transistor on the pre-strained semiconductor layer,
wherein a source/drain axis of the transistor is aligned along
10 the crystal orientation of the pre-strained semiconductor
layer.

16. The method of claim 15, wherein the crystal orientation of the pre-
strained semiconductor layer is determined to enhance current transport
15 capability of a PMOS transistor.

17. The method of claim 15, wherein the semiconductor device is a silicon-
on-insulator device.

20 18. The method of claim 15, wherein providing a pre-strained semiconductor
layer further comprises:

providing an at least partially relaxed silicon-germanium layer; and
forming a silicon layer on the at least partially relaxed silicon-
25 germanium layer from the pre-strained semiconductor layer.

19. The method of claim 15, wherein defining a crystal orientation of the
semiconductor substrate comprises defining a $\langle 110 \rangle$ direction of the
semiconductor substrate.

20. The method of claim 15, wherein defining a crystal orientation of the pre-strained semiconductor layer comprises defining a $\langle 100 \rangle$ direction of the pre-strained semiconductor layer.

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21. The method of claim 20, wherein forming a transistor on the pre-strained semiconductor layer comprises aligning a source/drain axis of the transistor along the $\langle 100 \rangle$ direction of the pre-strained semiconductor layer.

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22. The method of claim 21, wherein forming a transistor on the pre-strained semiconductor layer comprises aligning a source/drain axis of the transistor perpendicular to the $\langle 100 \rangle$ direction of the pre-strained semiconductor layer.

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23. The method of claim 15, further comprising cleaving the semiconductor device through the pre-strained semiconductor layer.

24. The method of claim 15, further comprising polishing the pre-strained semiconductor layer after cleaving.

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25. A semiconductor device comprising:

a semiconductor substrate having a first crystal orientation;
an insulating layer formed on a surface of the semiconductor
substrate; and

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a pre-strained semiconductor layer bonded to the insulating layer,
the pre-strained semiconductor layer having transistors
formed thereon, wherein channel regions of the transistors

are aligned with a second crystal orientation, the second crystal orientation being different than the first crystal orientation.

- 5 26. The semiconductor device of claim 25, wherein the pre-strained semiconductor layer is in a tensile stress state.
- 10 27. The semiconductor device of claim 25, wherein the pre-strained semiconductor layer is formed by depositing a silicon layer on an at least partially relaxed silicon-germanium layer.
- 15 28. The semiconductor device of claim 25, wherein the second crystal orientation is along a natural cleave plane of the pre-strained semiconductor layer, and the first crystal orientation is aligned 45 degrees from the second crystal orientation.
- 20 29. The semiconductor device of claim 25, wherein the second crystal orientation is rotated 45 degrees from the first crystal orientation.
- 25 30. The semiconductor device of claim 25, wherein the channel regions of the transistors are aligned in a $\langle 100 \rangle$ direction.
31. The semiconductor device of claim 25, wherein the semiconductor device is a silicon-on-insulator device.